Design and Implementation of GNSS Disciplined Clock Based on Unbiased FIR Filter

Qian Liu[1,2], Junliang Liu[1], Jianfeng Wu[1], Yan Xing[1] and Haili Wang [3]
[1]*National Time Service Center, Chinese Academy of Sciences, Xi'an, China*
[2] *University of the Chinese Academy of Sciences, Beijing, China*
[3]*ChinaXi'an Satellite Control Center, Xi'an, China*
{liujunliang, wujianfeng}@ntsc.ac.cn, liuqian115@mails.ucas.ac.cn

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Abstract: The disciplined clock system aiming at providing frequency signal with excellent frequency stability, which combines the well short-term frequency stability of the oven controlled crystal oscillator(OXCO) with the excellent long-term frequency stability of the one pulse per second (1PPS) output of the global navigation satellite system (GNSS) receiver. Based on the phase locked loop(PLL) structure, a disciplined clock system mainly consisting of 3 parts has been designed, the clockbias information is get from the UBX protocol generating by the Ublox receiver, and the unbiased finite impulse response(FIR) filter having a good performance is used as a loop filter. Some experiments are carried out, and it shows that the Allan variance of frequency stability of disciplined clock has been improved 2 orders and reached to 1.97×10^{-11} @10000s compared to the OXCO whose frequency stability is 1.56×10^{-9} @10000s.

1 INTRODUCTION

The use of 1PPS signal to discipline the local OCXO on the relevant research carried out in foreign countries Earlier. In view of the sawtooth error of the 1PPS signal and local crystal oscillator frequency deviation, aging and frequency offset, this problem was originally proposed in 1982 and Allan and Barnes proposed using Kalman filter to solve the problem. In 1999, Yuriy S. Shmaliy found that the Kalman estimates may become biased when the noise is not a Gaussian noise. Yuriy S. Shmaliy studied a variety of ways to weaken these errors. In 2002, he proposed the Unbiased sliding average filter to reduce the noise and found that this method is better than the third-order Kalman filter. However, it is possible that the OXCO will drift due to other factors such as temperature. In this case, the filter becomes less effective. In 2003 Nigel C. Helsby proposed the use of balanced mixers and DDS to achieve local oscillator frequency drift calibration, making frequency stability to achieve greater improvement. In 2006, Yuriy S. Shmaliy proposed an unbiased FIR filter, which is very effective for the TIE model. For noise signals that are not Gaussian white noises, it also has a better inhibitory effect.

In this paper, using the unbiased FIR filter method as a loop filter, which is based on PLL structure, and getting the information of clockbias by the Ublox UBX protocol. The results obtained using the symmetricom 5125A. In what follows, Section 2 presents the system design of the disciplined clock including the detailed description of each component. Section 3 describes the experimental platform and the measurement results. Finally, conclusions are given at Section 4.

2 DISCIPLINED CLOCK SYSTEM DESIGN

The disciplined clock system is essentially a phase-locked loop which consists of three parts, including the phase detector (PD), the voltage-controlled oscillator (VCO) and the loop filter (LP). The role of the phase-locked loop is to output a frequency signal synchronized with the frequency and phase of the input reference signal. In the synchronized state, the phase detector output phase difference between the input signal and the output signal is 0 or a constant. Its basic structure is shown in Fig.1,

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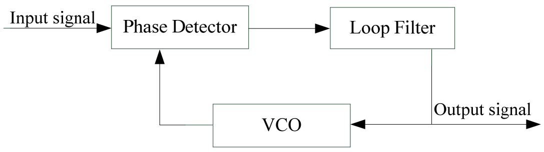

Figure 1: the structure of a phase-locked loop

The realization architecture is given in Fig.2.

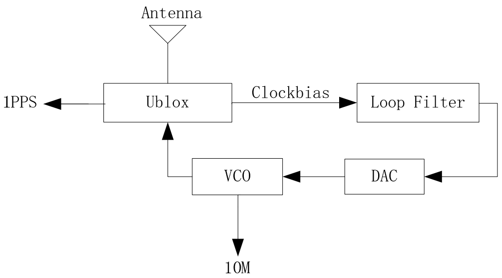

Figure 2: realization architecture of the disciplined clock

The Ublox provides accurate measurement of the external oscillator, and external interface has been equipped with in Ublox receiver to control the external oscillator. What's more, the Ublox can receive the GPS, GLONASS, BeiDou concurrently, and it integrates a low phase noise 30.72 MHz reference oscillator.The measurement of frequency and phase offset usually given in the UBX protocol, and the CPU can obtain information by the SPI/I2C.

Voltage control circuit is the most important part of the disciplined clock system which can adjust OCXO's voltage value. As shown in Fig.3., the system uses a DAC conversion chip, it is a 16-bit precision DA, DAC8811, providing -12V ~ 12V voltage control range.

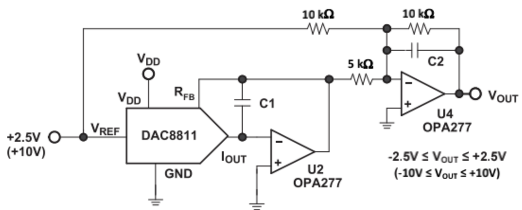

Figure 3: voltage control circuit

The output voltage is formed by

$$V_{out} = (\frac{D}{32768} - 1) \times V_{ref} \quad (1)$$

Where D is the D/A value of the D/A converter. Different OXCO's voltage and frequency deviation obey a certain function. At first, measuring the relationship data of the voltage-controlled voltage and frequency deviation of the OXCO. Then, fitting their approximate function using the principle of the least square method,. The relationship between the output frequency signal and the D/A value is expressed by

$$f_{oxco} = -0.0012 \times D + 39.6692 \quad (2)$$

Where D is the D/A value of the D/A converter and f_{oxco} is the frequency of the OXCO's output signal.

For the 16 bit D/A, the frequency resolution of the voltage control circuit is 0.0012Hz. The short-term frequency accuracy will be reach to 10^{-10} , the higher the accuracy, the frequency adjustment will be more accurate. however, the noise caused by the circuit board should be little.

For a loop filter in a PLL, the main purpose of which is to transfer a control signal to the VCO and to establish the dynamic characteristics of the loop. According to the OXCO frequency measurement model, the measurement error can be expanded to the Taylor series. Considering the characteristics of the OXCO itself, only the first three terms of the Taylor series are needed. The model expression is

$$x_1(n) = x_1(0) + x_2(0)\tau n + \frac{x_3(0)\tau^2 n^2}{2} + \varepsilon \quad (3)$$

Where n can be 0, 1, 2, 3, …, τ is the frequency measurement interval, $x_1(0)$ is the clock bias, $x_2(0)$ is an initial frequency offset of a local clock from the reference frequency, $x_3(0)$ is an initial frequency drift rate, ε is a random noise caused by the oscillator and environment.

Let

$$A(n) = \begin{bmatrix} 1 & \tau n & \tau^2 n^2 \\ 0 & 1 & \tau n \\ 0 & 0 & 1 \end{bmatrix} \quad (4)$$

And $\lambda(n) = [x_1(n)\ x_2(n)\ x_3(n)]^T$ is a vector of the clock states, $\xi(n) = [\xi_1(n)\ \xi_2(n)\ \xi_3(n)]^T$ is the observation vector, we have that

$$\lambda(n) = A(n)\lambda(0) + \varepsilon \quad (5)$$

$$\xi(n) = \lambda(n) + v(n) \quad (6)$$

$v(n)$ is a mean zero noise, and $v(n) >> \varepsilon$, and we need to derive $\hat{\lambda}(n) = [\hat{\lambda}_1(n)\ \hat{\lambda}_2(n)\ \hat{\lambda}_3(n)]^T$ the unbiased FIR estimator of the clock states, using the N points of the nearest past,

$$\hat{\lambda}(n) = \sum_{i=0}^{N-1} H(i)\xi(n-i) \quad (7)$$

$$H(i) = \begin{bmatrix} h_2(i) & 0 & 0 \\ 0 & h_1(i) & 0 \\ 0 & 0 & h_0(i) \end{bmatrix} \quad (8)$$

and the coefficients have the following properties:

$$h_l(i) = \begin{cases} h_l(i) & 0 \le i \le N-1 \\ 0 & otherwise \end{cases} \quad (9)$$

The block diagram of the unbiased FIR filter is illustrated in the Fig.4， the measurement $\xi_1(n)$ is filtered by the FIR $h_2(i)$ and the output $\hat{x}_1(n)$ represents the unbiased estimate of clockbias, the output $\hat{x}_2(n)$ represents the unbiased estimate of the derivative of $\hat{x}_1(n)$,and so forth.

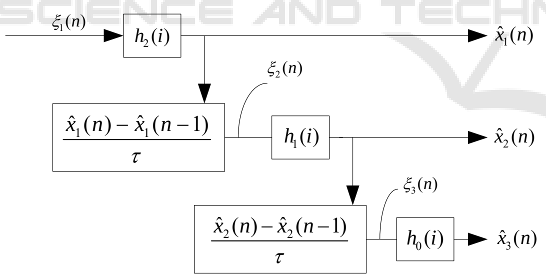

Figure 4: the block diagram of unbiased FIR filter

$$\hat{x}_1(n) = \sum_{i=0}^{N_2-1} h_2(i)\xi(n-i)$$
$$\hat{x}_2(n) = \frac{1}{\tau}\sum_{j=0}^{N_1-1} h_1(j)[\hat{x}_1(n-j) - \hat{x}_1(n-j-1)] \quad (10)$$
$$\hat{x}_3(n) = \frac{1}{\tau N_0}\sum_{k=0}^{N_0-1} h_0(k)[\hat{x}_2(n-k) - \hat{x}_2(n-k-1)]$$

And the first estimate $\hat{x}_1(n)$ appears at $N_2 - 1$, the first estimate $\hat{x}_2(n)$ appears at $N_1 + N_2 - 1$, and the first estimate $\hat{x}_3(n)$ appears at $N_0 + N_1 + N_2 - 1$, where the FIRs $h_0(i)$, $h_1(i)$ and $h_2(i)$ are given respectively

$$h_0(i) = \frac{1}{N} \quad (11)$$

$$h_1(i) = \frac{2(2N-1) - 6i}{N(N+1)} \quad (12)$$

$$h_2(i) = \frac{3(3N^2 - 3N + 2) - 18(2N-1)i + 30i^2}{N(N+1)(N+2)} \quad (13)$$

3 EXPERIMENTAL PLATFORM AND EXPERIMENTAL RESULTS

3.1 Experimental Platform

To evaluate the performance of the output frequency of the circuit board, the measurement set is organized as shown in Fig.5,

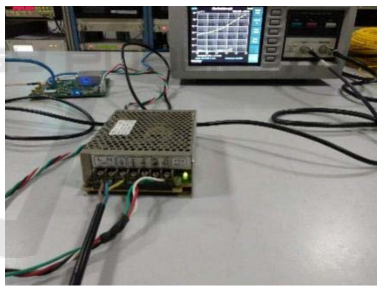

Figure 5:the measurement set

The 10MHz frequency signal of the disciplined clock goes to the first input of the Phase noise analyser symmetricom 5125A which has great phase noise performance, -140dBc/Hz at a 1Hz offset (10MHz fundamental), makes it the perfect solution to characterize the lowest noise frequency reference available, and the reference signal is the 10MHz signal frequency in NTSC (National Time Service Center in China) going to the second input of the symmetricom 5125A.

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3.2 Frequency stability analysis

After 2 days' measurement, the Allan deviation results of each component are shown in Fig.6 and Fig.7.

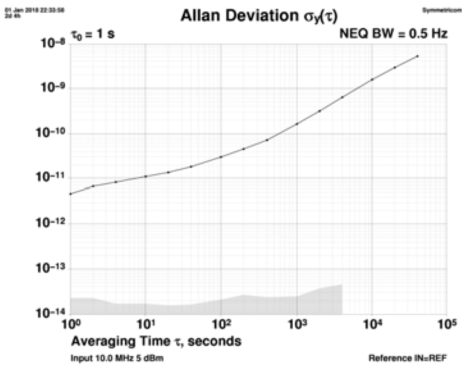

Figure 6: the Allan deviation of the OXCO before disciplined

In Fig.6., The curve goes up with τ due to the frequency drift which is mainly caused by aging and the temperature drift.

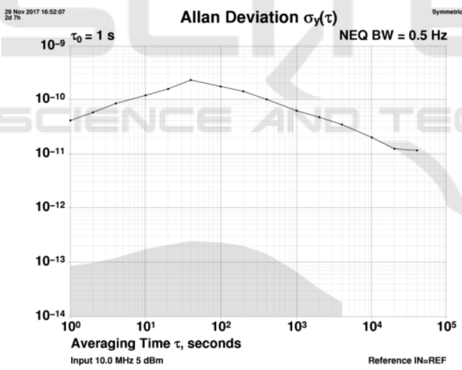

Figure 7: the Allan deviation of the OXCO after disciplined

In Fig.7., the curve starts to go down when $\tau > 40s$ owing to the GNSS signal having an excellent long-term frequency stability.

Table 1: the Allan deviation of the OXCO before disciplined and after disciplined.

	$\tau = 1s$	$\tau = 10s$	$\tau = 10000s$
Before disciplined	4.736×10^{-12}	1.120×10^{-11}	1.56×10^{-9}
After disciplined	4.040×10^{-11}	1.178×10^{-10}	1.97×10^{-11}

To compare the Allan deviation of the OXCO before disciplined and after disciplined, presented in Table 1, and τ is the sampling interval. The short-term stability of the OXCO become worse, due to correcting frequency frequently, which cannot be avoided. However, the Allan variance of long-term frequency stability of OXCO has been improved 2 orders which is 1.56×10^{-9} @10000s before disciplined and then become 1.97×10^{-11} @10000s after disciplined.

4. CONCLUSIONS

The paper has presented a method to discipline the local clock using the unbiased FIR filter as a loop filter in the PLL, and getting the information of clockbias by the UBX protocol. The experiment shows that it can improve the frequency stability of crystal oscillator about 2 orders.

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APPENDIX

1PPS	1 pulse per second
GNSS	global navigation satellite system
GPS	global positioning system (U.S.)
NTSC	national time service center
OCXO	oven controlled crystal oscillator
FIR	finite impulse response
GLONASS	global navigation satellite system

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