The Design of a Fully Differential Capacitive Pressure Sensor with Unbalanced Parasitic Input Capacitances in 130nm CMOS Technology

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Abstract: A switched capacitor amplifier for measuring absolute pressure with a micro-machined capacitive pressure sensor using correlated double sampling has been designed in 130nm CMOS technology. The switched capacitor amplifier design uses a combination of correlated double sampling, input offset cancellation, and output offset cancellation to help reject $\frac{1}{f}$ noise and DC offset mismatch. A method for sizing the operational transconductance amplifier (OTA) components according to the system noise, accuracy, and bandwidth requirements is presented.

1 INTRODUCTION

This paper will describe the design of a system for measuring absolute pressure with a micro-machined capacitive pressure sensor. The design will be used in a blood pressure sensing wireless medical implant (Buhk et al., 2010) which will be permanently implanted inside an artery and powered through RF inductive wireless power transmission (Bradford et al., 2012).

The wireless implant will be placed inside of the artery whose pressure it should monitor, necessitating small size and low power consumption. The goal of the whole design process is to create a system which delivers the required sensor resolution, at the necessary noise levels, with the lowest power budget.

2 CAPACITIVE PRESSURE SENSOR

The theory of operation of a capacitive pressure sensor is based upon the general formula for capacitance

$$C = \frac{\varepsilon A}{d}$$

where ε is the relative permittivity, A is the area, and d is the separation between the capacitor's two electrode plates. When pressure is applied to the sensor, the electrode plates are squeezed together resulting in a larger capacitance value. The circuit which is used to stimulate the capacitive pressure sensor is the capacitive bridge from Figure 1, and everywhere throughout the system, the switches $S0$ and $S1$ are activated by non-overlapping clocks.

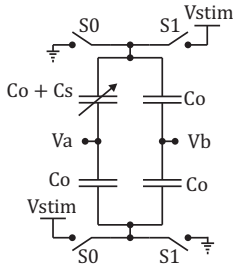

Figure 1: The capacitive pressure sensor as part of a capacitive bridge.

The pressure sensing capacitor has a nominal capacitance C_0 and a sense capacitance C_s which is a linear function of the applied pressure. Using superposition theory, the change in voltage at node V_a generated by the switch transition $S_0 \rightarrow S_1$ can be calculated as a function of V_{stim} (1).

$$\Delta V_{ab} = V_{stim} \frac{C_s}{C_s + 2C_0} \tag{1}$$

The maximum expected input signal peak-peak swing $\Delta V_{ab_{max_{pp}}}$ can be calculated by substituting C_s with the maximum expected peak-peak capacitances of $\pm\frac{C_{s_{max}}}{2}$. For the output swing, if V_{DD} is the maximum output voltage level, $V_{out_{pp}} = 2\,V_{DD}$, and the

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required closed loop gain (2) can be used to find the value for the feedback capacitance C_f in Figure 2.

$$A_{cl} = \frac{2\,V_{stim}}{\Delta V_{ab_{maxpp}}} = \frac{2\,C_0}{C_f} \quad (2)$$

$$C_f = \frac{2C_0}{A_{cl}} \quad (3)$$

3 SC NOISE ANALYSIS

The SC amplifier is a fully differential SC amplifier with input and output offset compensation (Fig. 2) (Enz and Temes, 1996). During SC switch phase *S*0, the amplifier is in unity gain configuration where the OTA's DC offset voltage V_{os} and the system noise voltage $V_{x_{ab}S0noise}$ are sampled across the nodes $V_{x_{ab}}$ (4). During phase *S*1, V_{os}, the system noise voltage $V_{x_{ab}S1noise}$, and the capacitance to voltage conversion result, ΔV_{ab}, are applied across $V_{x_{ab}}$ (5).

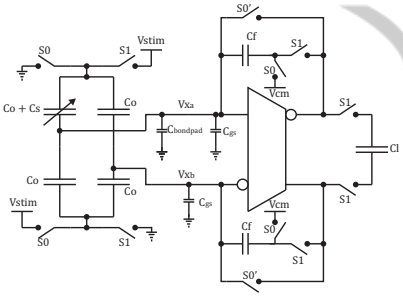

Figure 2: Schematic of the capacitive bridge and the SC amplifier with associated parasitic capacitances.

$$V_{x_{ab}S0} = V_{os} + V_{x_{ab}S0noise} \quad (4)$$

$$V_{x_{ab}S1} = V_{os} + V_{x_{ab}S1noise} + \Delta V_{ab} \quad (5)$$

$$V_{x_{ab}S1-S0} = \Delta V_a + V_{x_{ab}S0noise} + V_{x_{ab}S1noise} \quad (6)$$

3.1 SC Noise Analysis for Phase *S*0

To determine the noise from switch phase *S*0, the circuit from Fig. 2 can be reduced to the circuit in Figure 3.

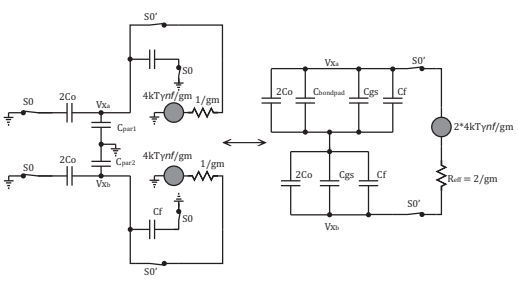

Figure 3: Schematic of the SC amplifier during phase S0.

The circuit from Figure 3 has the OTA in unity gain feedback which results in a differential thermal output noise voltage which is equal to the sum of the OTA's input devices' input referred noise voltages (7).

$$V^2_{noise_{OTA}} = 2 * \left(4kT\frac{\gamma_{in}}{gm}\right) nf \quad (7)$$

The γ factor for this 130 nm CMOS technology has been determined by performing Spectre small signal noise analysis simulations (Figure 4). The simulation results show that the γ factor has a strong correlation to the MOSFET's transconductance efficiency $\eta_{gm} = \frac{gm}{I_d}$.

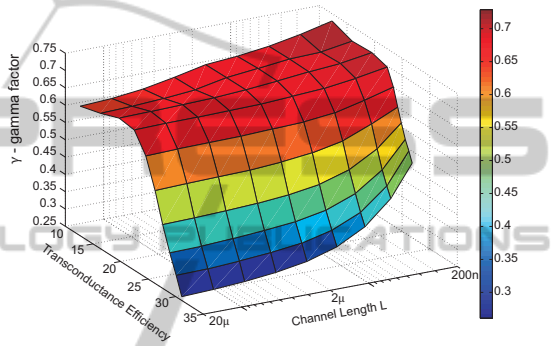

Figure 4: Plot of the γ noise factor against the channel length and transconductance efficiency. The data was collected by performing SPICE small signal noise simulations on a 130 nm CMOS technology NMOS device.

From (7), *nf* is the noise factor which scales the OTA's input MOSFET device's input referred noise up to the total output noise voltage of the OTA (Sec. 4.1). The OTA's thermal output noise is bandwidth limited by the noise equivalent bandwidth (NEB) (9) (Baker, 2011).

$$NEB = GBW\frac{\pi}{2}$$

$$GBW = \frac{gm}{2\pi(2\,C_{eq})} \quad (8)$$

$$NEB = \frac{gm}{4(2\,C_{eq})} \quad (9)$$

The parameter C_{eq} is the differential load capacitance across the outputs of the OTA during switching phase *S*0. At the nominal pressure where $C_s = 0$, C_{eq} can be derived as (10).

$$C_{eq_a} = 2C_0 + C_{par1} + C_f$$

$$C_{eq_b} = 2C_0 + C_{par2} + C_f$$

$$C_{eq} = \frac{C_{eq_a}C_{eq_b}}{C_{eq_a} + C_{eq_b}} \quad (10)$$

The OTA input referred thermal noise, (7), multiplied by the NEB (9) which is bandwidth-limited by C_{eq} (10) results in a noise voltage across $V_{x_{ab}}$ of (11)

$$V^2_{x_{ab}S0_{noise}} = \frac{kT}{C_{eq}}\gamma_{in}nf \tag{11}$$

After the SC amplifier has switched to phase $S1$, the noise charge gets transferred to the output nodes as a function of the feedback factor F (12).

$$V_{out} = \frac{V_{x_{ab}}}{F} \tag{12}$$

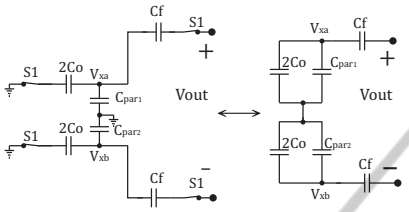

Figure 5: Equivalent schematic for determining the feedback factor (13).

From Figure 5, F is the transfer function from the OTA's output to its input (13).

$$F = \frac{V_{x_{ab}}}{V_{out}} = \frac{\frac{C_f}{2}}{\frac{C_f}{2} + \frac{(2C_0+C_{par1})(2C_0+C_{par2})}{(2C_0+C_{par1})+(2C_0+C_{par2})}} \tag{13}$$

The final output noise contribution from phase $S0$ is found by combining (11), (12), and (13) into (14).

$$V^2_{out_{noise_{S0}}} = \frac{kT}{C_{eq}}\frac{\gamma_{in}nf}{F^2} \tag{14}$$

3.2 SC Noise Analysis for Phase *S*1

The switches in the feedback and output path of the circuit can be ignored if their resistance $R_{sw} \ll \frac{1}{gm\,F}$ (Murmann, 2012). The two remaining $S1$ noise sources are the input switch resistive noise and the OTA input referred noise voltage (Figure 6).

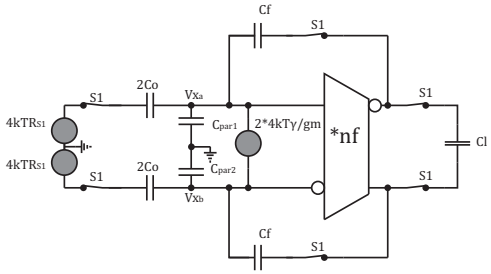

Figure 6: Schematic of the SC amplifier during phase S1.

First, considering the switch input noise, the S1 switch noise generators produce a differential noise voltage $V^2_{noise_{input}} = 2 * 4kTR_{S1}$. This noise voltage is amplified by the closed loop gain of the amplifier, A_{cl}, and it is energy limited by the NEB resulting in a total input switch noise contribution of (15).

$$\begin{aligned} V^2_{out_{noise_{RS1}}} &= (2 * 4kTR_{S1})\, A^2_{cl}\, NEB \\ V^2_{out_{noise_{RS1}}} &= \frac{kT}{C_{leff}}\, A^2_{cl}\, R_{S1}\, gm\, F \end{aligned} \tag{15}$$

The other noise contributor for phase $S1$ is the OTA's thermal noise. As it was for switching phase $S0$, the input referred thermal noise of the OTA is (7), and the output noise is the input noise divided by F and bounded by the NEB (16).

$$\begin{aligned} V^2_{onoise_{OTA}} &= 8kT\frac{\gamma_{in}\,nf}{gm}\frac{1}{F^2}\frac{gm\,F}{8\,C_{leff}} \\ V^2_{onoise_{OTA}} &= \frac{kT}{C_{leff}}\frac{\gamma_{in}\,nf}{F} \end{aligned} \tag{16}$$

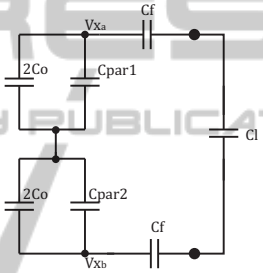

Figure 7: The circuit used to determine the OTA effective output capacitance C_{leff}.

Figure 7 can be used to calculate C_{leff}, and after a bit of algebra, C_{leff} can be expressed as (17).

$$C_{leff} = C_l + \frac{C_f}{2}(1-F) \tag{17}$$

Summing the two noises (15) and (16) results in (18), which is the total SC phase $S1$ noise contribution.

$$V^2_{noise_{S1}} = \frac{kT}{C_{leff}}\left(A^2_{cl}\, R_{S1}\, gm\, F + \frac{\gamma_{in}\,nf}{F}\right) \tag{18}$$

From (18), if the following condition is fulfilled:

$$A^2_{cl}\, R_{S1}\, gm\, F \ll \frac{\gamma_{in}nf}{F}$$

then it is safe to consider only the OTA's noise contribution for the phase $S1$ noise. With this simplification, (14) and (16) can be summed together to give the total system noise (19).

$$V^2_{noise_{total}} = kT\frac{\gamma_{in}nf}{F}\left(\frac{1}{C_{eq}\,F} + \frac{1}{C_{leff}}\right) \tag{19}$$

4 NOISE FACTOR AND C*l*

For an ADC with an N bit resolution, the total allowable error is (20).

$$\varepsilon^2_{total} = \frac{V^2_{signal_{rms}}}{10^{\frac{6.02*N+1.76}{10}}} \quad (20)$$

$$\varepsilon_{total_{pp}} = \sqrt{\varepsilon^2_{total} 2\sqrt{2}} \quad (21)$$

Eq. (21) gives the peak-peak noise error budget for the system. The required thermal noise SNR is increased by a few dB, denoted by SNR_{extra} in (22), so that only a fraction of the total error will be given to noise (23).

$$\varepsilon^2_{noise_{rms}} = \frac{V^2_{signal_{rms}}}{10^{\frac{6.02*N+1.76+SNR_{extra}}{10}}} \quad (22)$$

$$noise\ fraction = 10^{-\left(\frac{SNR_{extra}}{10}\right)} \quad (23)$$

Choosing a value for C_{gs} based upon its expected length and width, then C_{eq} and F can be solved. (19) and (22) can be combined to form (24) and (25), from which the nf or the C_{leff} can be determined based on the circuit noise requirements.

$$nf = \frac{\varepsilon^2_{noise} F}{kT\gamma_{in}\left(\frac{1}{C_{eq}F} + \frac{1}{C_{leff}}\right)} \quad (24)$$

$$C_{leff} = \frac{kT\gamma_{in} nf\, C_{eq} F}{\varepsilon^2_{noise} F^2\, C_{eq} - kT\gamma_{in} nf} \quad (25)$$

4.1 Noise Factor Determination

The total OTA noise is a summation of the $4kT\gamma\, gm$ noise currents to the output (26), and the OTA noise factor, nf, input refers the total output noise to the input device gm by dividing by gm_1^2 (27).

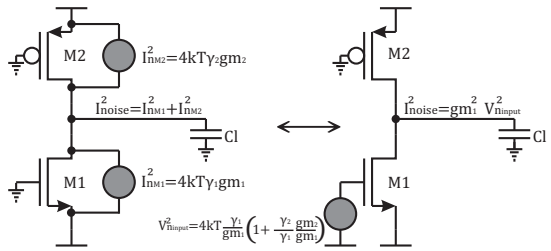

Figure 8: Input referred system noise current.

$$I^2_{noise_{out}} = 4kT\left(\gamma_1 gm_1 + \gamma_2 gm_2\right) \quad (26)$$

$$V^2_{noise_{input}} = 4kT\frac{\gamma_1}{gm_1}\left(1+\frac{\gamma_2 gm_2}{\gamma_1 gm_1}\right) \quad (27)$$

$$nf = \left(1+\frac{\gamma_2 gm_2}{\gamma_1 gm_1}\right) \quad (28)$$

The nf design parameter can be expressed in terms of transconductance efficiency values (29), normalized to the input device drain current (30).

$$\eta_{gm} = \frac{gm}{I_d} \quad (29)$$

$$nf = 1+\frac{I_{d_2}}{I_{d_1}}\frac{\gamma_2 \eta_{gm_2}}{\gamma_1 \eta_{gm_1}} \quad (30)$$

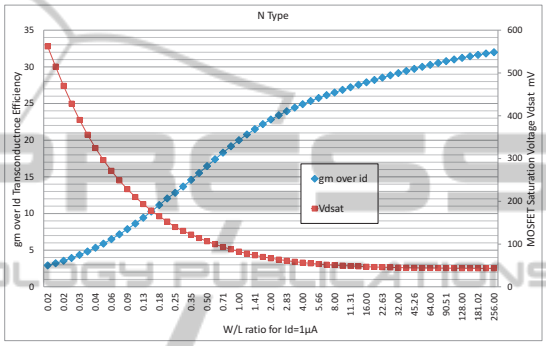

Figure 9: Spectre simulation results sweeping channel $\frac{W}{L}$ ratio with fixed $I_d = 1\mu A$ of a 130nm N-type MOSFET.

Using the data from Figures 4 and 9, γ and η_{gm} values can be chosen which allows the amplifier to meet the nf and output swing requirements.

4.2 Gain, Settling and *gm*

The remaining error available for the settling is (31), and the gain and bandwidth of the amplifier must be great enough to settle the output to within ε_{settle} in only $\frac{1}{2}$ period of the SC amplifier clock. The settling error is comprised of the static error, ε_{static} (33), and the dynamic error, $\varepsilon_{dynamic}$ (34).

$$\varepsilon_{settling} = \varepsilon_{total_{pp}}\left(1-10^{-\left(\frac{SNR_{extra}}{10}\right)}\right) \quad (31)$$

The amplifier's loop transfer function T_0 (32) determines the static error (33) of the analog conversion, where A_0 is the open loop gain of the amplifier.

$$T_0 = A_0\, F \quad (32)$$

$$\varepsilon_{static} = \frac{1}{T_0}$$

$$\varepsilon_{static} = \frac{1}{A_0\, F} \quad (33)$$

The dynamic error of the amplifier is determined using the amount of time available to settle, t_s, and the

$\tau = R_{OTA}C_{load}$ time constant of the OTA (34). At low SC clock speeds, t_s is $\frac{1}{2}$ the SC system clock period, R_{OTA} is the effective resistance. $\frac{1}{gm\,F}$, of the amplifier, and $C_{load} = 2\,C_{leff}$ is the effective output capacitance of the OTA output node.

$$\begin{aligned} \varepsilon_{dynamic} &= e^{-\frac{t_s}{\tau}} \\ \varepsilon_{dynamic} &= e^{-\frac{gm\,F}{4\,f_{sc}C_{leff}}} \end{aligned} \quad (34)$$

Equations (33) and (34) can be combined to form (35).

$$\begin{aligned} \varepsilon_{settle} &= \varepsilon_{static} + \varepsilon_{dynamic} \\ gm &= -\frac{4\,C_{leff}\,f_{sc}}{F} ln\left(\varepsilon_{settling} - \varepsilon_{static}\right) \end{aligned} \quad (35)$$

For *gm* to be real and finite (36) must be true.

$$A_0 > \frac{1}{\varepsilon_{settling}\,F} \quad (36)$$

Solving (35) for minimum open loop gain results in infinite *gm*, and solving for minimum *gm* requires infinite A_0 (Fig. 11). Increasing A_0 by a few dB quickly results in near minimum *gm* requirements. With *gm* from (35), and the input transistor η_{gm} ratio for the required *nf*, then the drain current through each input device is (37).

$$I_d = \frac{gm}{\eta_{gm}} \quad (37)$$

With I_d and η_{gm}, Figure 9 can be used size the $\frac{W}{L}$ ratio for each transistor.

5 SC AMPLIFIER DESIGN EXAMPLES

The system has been designed to measure absolute pressure with the Protron-Mikrotechnik capacitive absolute pressure sensor using a 1.2 VDC stimulation voltage at the human body temperature of 38°C. Table 1 lists the design parameters which are to be used in the SC amplifier design.

Three different designs have been created with the Cadence Design Framework using the UMC 130nm technology, and the design variables are listed in Table 2. The amplifier architecture which is used for each design is the gain boosted folded cascode amplifier from Figure 10 (Bradford et al., 2013) which is able to provide 102 dB of gain over the required $\pm 850\,mV$ of output swing. Eq. (38) is used to select the γ and $\eta_g m$ values for the amplifier.

$$nf = 1 + \left(\frac{I_{d_2}}{I_{d_1}}\right)\frac{\gamma_2\eta_{gm_2}}{\gamma_1\eta_{gm_1}} + \left(\frac{I_{d_5}}{I_{d_1}}\right)\frac{\gamma_5\eta_{gm_5}}{\gamma_1\eta_{gm_1}} \quad (38)$$

Plotting (35) for $f_{sc} = 4kHz$, Figure 11, allows a system *gm* to be selected based on an open loop gain of $A_0 = 102\,dB$.

Table 1: Pressure sensor system design constants.

Temperature		38°C
$2\,C_0$		12.0 pF
$C_{swing_{pp}}$		1.6 pF
$V_{ab_{max_{pp}}}$	(1)	160 mV
$V_{out_{pp}}$		2.4 V
A_{cl}	(2)	15 $\frac{V}{V}$
C_f	(3)	800 fF
$C_{bond\,pad}$		5.5 pF
C_l		4.6 pF
V_{stim}		1.2 VDC
ε_{total}	(20)	1.172 mV

Table 2: CDS system design values.

f_{sc}		4ksps	40ksps	400ksps
C_{gs}		100fF	500fF	1.5pF
C_{eq}	(10)	7.58pF	7.79pF	8.3pF
F	(13)	$0.053\frac{V}{V}$	$0.051\frac{V}{V}$	$0.048\frac{V}{V}$
C_{leff}	(17)	4.98pF	4.98pF	4.99pF
SNR_{extra}	(22)	2.2 dB	2.1dB	2.1dB
$\varepsilon_{noise_{rms}}$	(22)	522 μV	529μV	529 μV
$\varepsilon_{settling}$	(31)	452 μV	436μV	420u μV
nf_{max}	(24)	3.62	3.60	2.69
gm_{min}	(35)	11.6 μS	120 μS	1.282 mS
$A_{0_{min}}$	(36)	92.4dB	93.0dB	98.9dB
$\eta_{gm_{in}}$	Fig. 9	28	28	25
γ_{in}	Fig. 4	0.35	0.35	0.45
$\eta_{gm_{load}}$	Fig. 9	14	14	14
γ_{load}	Fig. 4	0.6	0.6	0.6
nf	(38)	3.57	3.57	2.6
A_0	Fig. 11	102dB	102dB	102dB
gm	Fig. 11	12.3μS	126 μS	1.364mS
I_d	(37)	440 nA	4.29 μA	54.6 μA

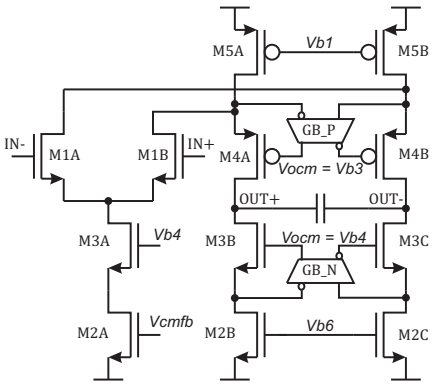

Figure 10: The gain boosted folded cascode amplifier.

5.1 Amplifier Design Verification

DC simulations are used to fine tune the transistor dimensions until they have the desired η_{gm} values.

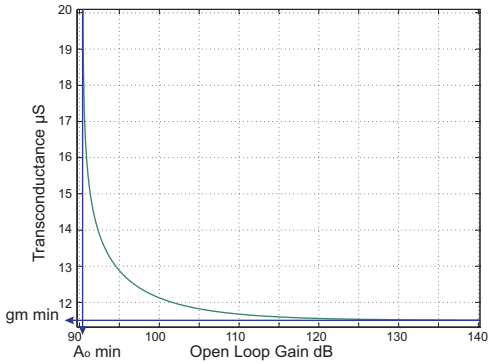

Figure 11: Plot of gm versus A_0 from (35) for $f_{sc} = 4kHz$ showing asymptotic behavior at minimum *gm* and minimum A_0.

Then, two different analyses, ac and pss/pnoise, are performed on each of the three amplifiers. The ac analysis is used to find the amplifier's GBW, and the pss/noise is used to verify the $V^2_{noise_{rms}}$ of the circuit. The three amplifiers are simulated using the exact device η_{gm} and I_d values listed in Table 2 without any further optimizations, and the pss/noise simulation is performed as per the guidelines documented in (Murmann, 2012).

Table 3: Spectre noise analysis simulation results.

f_{sc}	4 kHz	40 kHz	400 kHz
GBW (8)	196 kHz	2.013MHz	21.79 MHz
$GBW_{simulation}$	206.5 kHz	2.086 MHz	22.32 MHz
$\varepsilon_{noise_{rms}}$ (22)	522 μV_{rms}	529 μV_{rms}	529 μV_{rms}
$V^2_{noise_{rms}simulation}$	487 μV_{rms}	507 μV_{rms}	547 μV_{rms}

6 CONCLUSIONS

This paper has presented a method for measuring a commercially available micro-machined capacitive pressure sensor with a switched capacitor amplifier using correlated double sampling. The SC amplifier, with its unbalanced input load capacitances, is analyzed for noise and bandwidth requirements. A method for designing the amplifier to meet the noise requirements as a function of the OTA noise factor *nf* and transconductance efficiency values, η_{gm}, has been presented. In addition to the noise requirements, a method for achieving the settling requirements as a function of the SC frequency and the system open loop gain has been presented. This method for amplifier design was implemented using the Cadence Design Framework II, and verified using various Cadence Virtuoso Spectre simulations over an operating frequency range spanning three decades from 4 kHz to 400 kHz.

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